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A 13-levels Module (K-Type) with two DC sources for Multilevel Inverters

E. Samadaei, M. Kaviani, K. Bertilsson

***Abstract*—This paper presents a new reconfiguration module for asymmetrical multilevel inverters in which the capacitors are used as the DC links to creates the levels for staircase waveforms. This configuration of multilevel converter makes a reduction in DC sources. On the other hand, it is possible to generate 13 levels with lower DC sources. The proposed module of multilevel inverter generates 13 levels with two unequal DC sources ($2V_{DC}$ and $1V_{DC}$). It also involves two chargeable capacitors and 14 semiconductor switches. The capacitors are self-charging without any extra circuit. The lower number of components makes it desirable to use in wide range of applications. The module is schematized as two back-to-back T-type inverters and some other switches around it. Also, it can be connected as cascade modular which lead to a modular topology with more voltage levels at higher voltages. The proposed module makes the inherent creation of the negative voltage levels without any additional circuit (such as H-bridge circuit). Nearest level control switching modulation (NLC) scheme is applied to achieve high quality sinusoidal output voltage. Simulations are executed in MATLAB/Simulink and a prototype is implemented in the power electronics laboratory which the simulation and experimental results show a good performance.**

***Index Terms*— asymmetric, capacitors, multilevel inverter, power electronics, self-charging, nearest level control switching**

I. INTRODUCTION

Multilevel inverters (MLIs) have been providing the reliable and high quality voltage source converters (VSC) to connect the DC power systems to the AC power systems. MLIs with different configurations are one of the interesting devices in power electronics area. The verity of configuration spreads them as a wide range application in power system, recently. The abilities of MLIs in medium/high power applications against two levels inverters make them leading converter in photovoltaic systems [1], HVDC for transmission line [2, 3], wind turbine [4], active power filer [5], drives systems [6, 7], electrical vehicle [8] and power grid [9]. MLIs have high resolution on the output voltage and low harmonic components because of a high number of output levels. They also have low stress on switches, modularity, and scalability due to cascade connection ability. Multilevel converters are introduced into Neutral Point Clamped (NPC) [10], Flying Capacitor (FC) [11], Cascade H-bridge (CHB) [12]. Unbalanced DC links and high stress on switches are the disadvantages of NPC and FC which are including huge capacitors. Therefore, CHB types are focused by researchers, and reduced numbers of components are targeted in the configuration of CHB topologies. This kind of topologies are comparable from different aspects such as the number of levels, the number of DC sources, the number of semiconductors, total standing voltage (TSV), the inherent creating of negative levels and etc. some reviewing studies are presented in [13-16] for last decade topologies. A DC source generates one level by two switches in [17] and make one module, together. The module can be connected in series to create more levels. Although all levels are positive levels and it needs an additional circuit to create negative levels. H-bridge is added to the series modules in [18] for staircase sinusoidal waveform (negative and positive half-cycles). The semiconductors in H-bridge circuits which create negative voltage levels, tolerate high switching stress. Generally, MLIs arrange different connections of semiconductor switches to synthesize several small voltage steps to form a staircase output waveform. Using lower components to produce higher output voltage levels are one of the important issues in the configuration of MLIs. The applying of unequal DC links is the best method to achieve this issue. Asymmetric multilevel inverters with unequal DC links present a new type of configuration which reduced the number of components along with higher output voltage levels. Modules are designed based on adding or subtracting of DC links by power electronics semiconductors. On another side, the stress on switches should be considered in asymmetric multilevel inverters due to unequal DC sources. The stress on switches is introduced with total standing voltage (TSV) which is a total highest voltage of each switch in off mood. [19, 20] introduced crossing switches for opposite polarity of DC links to generate more levels and dividing of stress on switches. Extended H-bridge with different amount of DC links is presented in [21, 22]. Higher levels in this topologies are along with stress on switches that needs higher rate semiconductor. Hybrid type topologies are proposed as another type of MLIs in [23]. [24, 25] introduced modules with low semiconductors with inherent negative levels based on the achieving of maximum levels from four DC sources.

Evolution of MLIs tends to reduce components, especially DC sources which are replaced with capacitors, recently. Suitable topology with mixed capacitors and DC sources can provide a

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sinusoidal voltage source. On the other hand, it can be achieved more output voltage levels with the same DC sources. [26- 29] redesigned the configuration of [11, 19] with capacitors to remove some DC sources. [30-33] use a single source to generate output levels, although the number of semiconductors has been increased and charging/discharging of capacitors and switches driving become complicated. Some other topologies are proposed with mixed DC sources and capacitors as the stair modular configurations ([34-36]), although H-bridge are applied in the circuits.

This paper presents an arrangement of semiconductor with mixed DC sources and capacitors as DC links to achieve maximum voltage levels from DC sources which improve economic implementation cost and power quality. This module uses just two unequal DC sources with the amount of $1V_{DC}$ and $2V_{DC}$ to generate 13 output voltage levels. On the other hand, an asymmetric multilevel module is introduced to produces 6 positive levels, 6 negative levels and zero level (totally 13 levels) without any additional circuit to create negative voltage levels. 14 power electronics switches and two capacitors are implemented in the proposed module. The module can be connected in series as cascade connection easily to produce more and higher output voltage levels. Proposed multilevel inverter illustrates in Section II including module description, switching patterns, self-charging and discharging capacitors without any additional circuit, cascade connection and comparison table with similar modules. Nearest level control (NLC) is implemented for switching modulation for cascade connection mode which is described in section III. Power losses are examined in sections IV. The Analysis of capacitors ripple is examined in section V. Simulation and experimental results are shown in sections VI and VII, respectively. Conclusions are presented in section VIII.

II. Proposed Module

Fig.1 shows a general conceptual diagram of multilevel inverters. A suitable designing of power converter can achieve maximum output levels from two DC sources. It is possible to use capacitors to create some extra DC links to get more levels than the expectation. In this kind of configuration, the charging path of capacitors should be provided in addition to the output levels paths. It would be interesting to do not using an additional circuit for the charging of capacitors. Then a smart designing for the multilevel inverter is presented as follow:

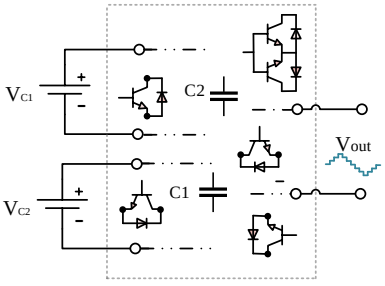

Fig.1 The general conceptual asymmetric MLIs with capacitors.

A. Module Configuration

There are two DC sources with different amounts as $1V_{DC}$ and $2V_{DC}$. Using unequal DC sources for asymmetric multilevel inverters products different number of output voltage levels by fewer semiconductors and lower harmonic components as well. It would be better to create two extra DC links with capacitors. It gives four DC links, totally. Fig.2 introduces the proposed module with a new component arrangement including 14 switches (8 unidirectional switches and 3 bidirectional switches), 14 diodes and 2 unequal DC source and 2 capacitors. This configuration generates six positive levels, six negative levels and zero level (13 levels totally). The shape of proposed topology is similar to Kite and it is named "K-Type" (Kite Type). The main concept of this circuit is creating different paths from different sides of a DC link to be connected to other DC links to creat negative levels in order to remove H-bridge. It is noticeable that DC source with $1V_{DC}$ charges the capacitor with $1V_{DC}$, and DC source with $2V_{DC}$ charges the capacitor with $2V_{DC}$ without any additional circuit. Fig.3 and Table 1 show switching patterns of the output levels in the proposed structure. The designing of the module and their switching paths are selected smartly in such a way that There are no positive pole of DC links on the anode side of diode to conduct. In addition, Fig.3 depicts the switching paths does not form any close loop for DC links. Thus, diodes polarity and bidirectional switches guarantee for suppressing of switches that short-circuiting will be not occurred in the module.

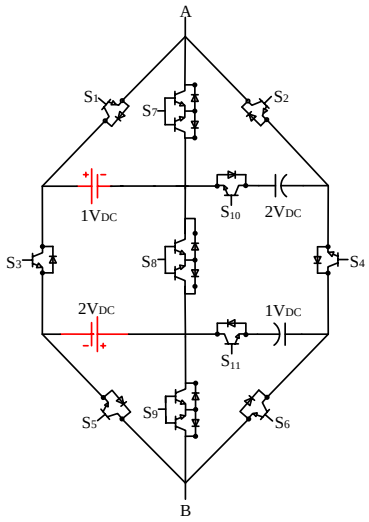

Fig. 2 The proposed module of multilevel inverter.

TABLE 1
SWITCHING TABLE

		S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}
	$6V_{DC}$	1	0	0	1	1	0	0	0	0	1	1
	$5V_{DC}$	0	0	0	1	1	0	1	0	0	1	1
	$4V_{DC}$	1	0	0	1	0	0	0	0	1	1	1
	$3V_{DC}$	1	0	0	0	1	0	0	1	0	0	0
	$2V_{DC}$	0	0	0	0	1	0	1	1	0	0	0
	$1V_{DC}$	1	0	0	0	0	0	0	1	1	0	0
Negative level	$-1V_{DC}$	0	0	1	0	1	0	1	0	0	0	0
	$-2V_{DC}$	1	0	1	0	0	0	0	0	1	0	0
	$-3V_{DC}$	0	0	1	0	0	0	1	0	1	0	0
	$-4V_{DC}$	0	0	1	0	0	1	1	0	0	0	1
	$-5V_{DC}$	0	1	1	0	0	0	0	0	1	1	0
	$-6V_{DC}$	0	1	1	0	0	1	0	0	0	1	1
Num. of turning on per 1-cycle		6	2	1	2	5	4	8	2	8	3	5

Table 1 indicates switch modes in each levels. Although, there are redundant paths for some levels from other DC links. Switch (S_1, S_7), (S_3, S_8) and (S_5, S_9) cannot be turned on at the same to

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prevent the short circuit between two DC sources. Number of switches turning on per one cycle for each switch is shown in last row of Table 1. Fig.4 shows schematic output voltage of the proposed inverter with the associated pulse pattern in one cycle of fundamental voltage. As shown in Fig.4, switches S_2, S_3, S_4 and S_8 are turned on in low frequency, which reduces switching losses. Other switches also operate in a reasonable switching frequency. Fig.4 also shows employed DC sources and capacitors for each level. Capacitors as the DC links are used in levels $\pm4^{th}$, $\pm5^{th}$ and $\pm6^{th}$. Consequently, two unequal DC sources with the proposed module create the 13-levels Module for Multilevel Inverters.

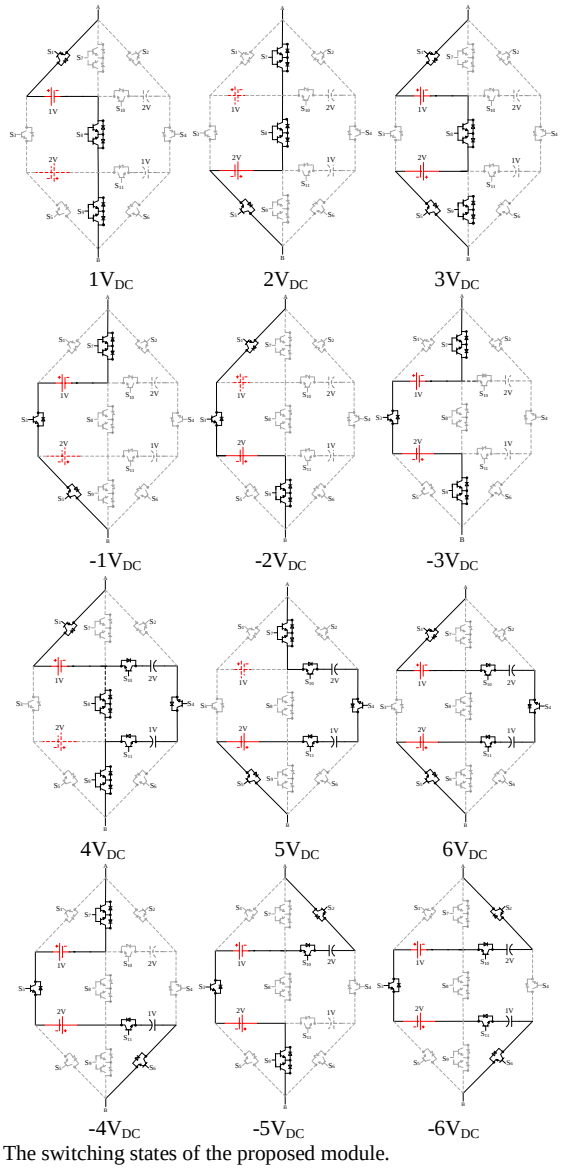


Fig. 3 The switching states of the proposed module.

Other feasibility of the module is the charging of capacitors without any additional circuit. The module is designed two loop paths for charging of DC links. Capacitors have been charged in level zero according to Fig.4. The path for charging of capacitors show in Fig.5 in which DC source with $1V_{DC}$ is charging 1Vc (Fig.5.a) and DC source with $2V_{DC}$ is charging 2Vc (Fig.5.b). According to Fig.4 the charging of the capacitors can happened in level zero. On the other hand, the capacitors are being charged for each half-cycle. the capacity of capacitors can be determined according to the application to keep the charging for one half-cycle and more. It is noticeable that the discharging of capacitors is in some levels of one cycle and also mixed DC sources and capacitors as the DC links cause the smooth behavior of capacitors.

The equations of the module are shown in Table 2. It determinates the number of the semiconductor, DC sources, capacitors and drivers based on the number of module units (n) in middle column and the number of output levels (N_L) in last column. Symbol "[]" is floor function.

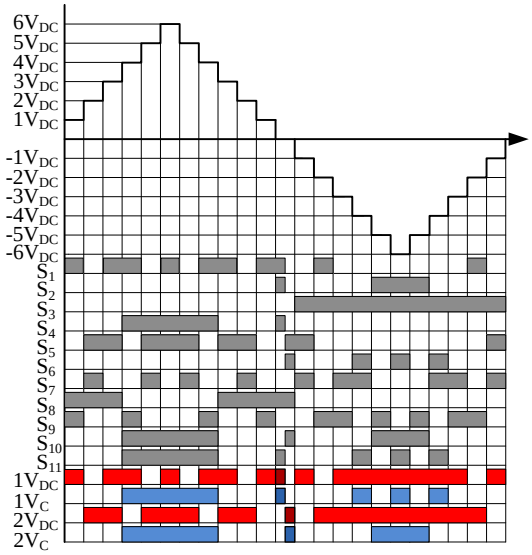
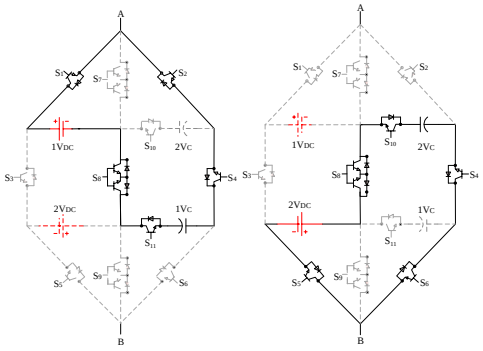


Fig.4 switching pattern/used DC links of proposed inverter in one-cycle.



(a) (b)

Fig. 5 The switching path for charging of capacitors in the proposed module, a) charging of 1Vc, b) charging of 2Vc.

TABLE 2
THE EQUATIONS OF PROPOSED MODULE

	Based on number of module units	Based on number of desired levels
Levels	12n+1	N_L
Number of Switches	14n	$14\left[\frac{N_L-2}{12}+1\right]$
Number of Diodes	14n	$14\left[\frac{N_L-2}{12}+1\right]$
Driver	9n	$11\left[\frac{N_L-2}{12}+1\right]$
DC sources	2n	$2\left[\frac{N_L-2}{12}+1\right]$
Capacitors	2n	$2\left[\frac{N_L-2}{12}+1\right]$
TSV	32n	$32\left[\frac{N_L-2}{12}+1\right]$

TSV (Total Standing Voltages) of the circuit is also presented

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in Table 2 as a parameter. According to Fig.3, the maximum magnitude of the blocking voltage of the power switches are examined for each switch. The sum of all blocking voltages for the switches are introduced as TSV.

The voltage standing on the switches and the circuit study in figures 6 and 7 in which Fig.6 illustrates total standing voltages for levels. It also divides the voltage standing on each switch for levels by different colors. Fig.6 confirms that the total standing voltage in levels is not more than $18xV_{DC}$ which illustrates good performance of proposed module. Fig.7 also depicts the voltage of switches on circle graph in which low voltage standing against total standing voltages is obvious in S_1, S_2, S_5, S_6, S_7, S_8, S_9, S_{10} and S_{11}.

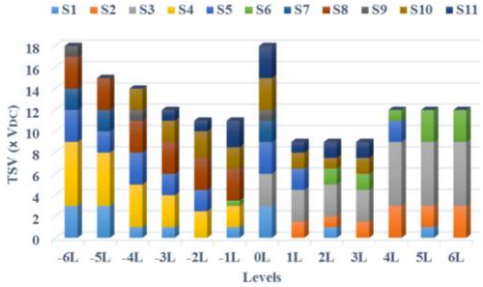

Fig.6 The bar graph of the voltage constraints on circuit for each levels.

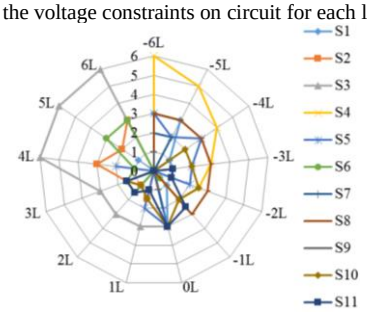

Fig.7 The circle graph of the voltage constraints on each switches.

B. Module Extension

The module can be connected in series to generate more output levels. Cascade connections would be applied when there are cumulative DC links applications such as solar PV farm. Fig.8 shows the cascade connection for two consecutive unit. The left unit (u_1) produces 0, $\pm1V_{DC}$, $\pm2V_{DC}$, $\pm3V_{DC}$, $\pm4V_{DC}$, $\pm5V_{DC}$ and $\pm6V_{DC}$. For the right unit (u_2), two strategies can be considered as two modes. Table 3 illustrates output levels of units for cascade connections States:

TABLE 3
OUTPUT LEVELS OF UNITS FOR CASCADE CONNECTIONS STATES

Unit 1 (u1)	**Unit 2 (u2)**	
	Mode.I	Mode.II
$Vu1=1V_{DC}$	Vu2, V_{L2}= the amount of DC links same as pervious unit,	Vu2=total number of levels in pervious units, $V_{L2}=2xVu$,
$V_{L1}=2V_{DC}$	$Vu2=1V_{DC}$ $V_{L2}=2V_{DC}$	$Vu2=13V_{DC}$ $V_{L2}=26V_{DC}$
Output levels: 0 $\pm1V_{DC}$ $\pm2V_{DC}$ $\pm3V_{DC}$ $\pm4V_{DC}$ $\pm5V_{DC}$, $\pm6V_{DC}$	Output levels: 0 $\pm1V_{DC}$, $\pm2V_{DC}$ $\pm3V_{DC}$ $\pm4V_{DC}$ $\pm5V_{DC}$ $\pm6V_{DC}$	Output levels: 0 $\pm13V_{DC}$ $\pm26V_{DC}$ $\pm39V_{DC}$ $\pm52V_{DC}$ $\pm65V_{DC}$, $\pm78V_{DC}$

In mode.I, the complex of unit 1 and unit 2, creates 25 levels (12 positive levels, 12 negative levels and zero level) as Table 4 and also The complex of unit 1 and unit 2 in mode.II, creates 169 levels (84 positive levels, 84 negative levels and zero level) as Table 5. In Table 4 and 5, $u1=\frac{V_{A1B1}}{V_{DC}}$, $u2=\frac{V_{A2B2}}{V_{DC}}$. It can be extended for several units. This feature of the proposed module can be created some redundant paths in mode.I as shown in Table 4.

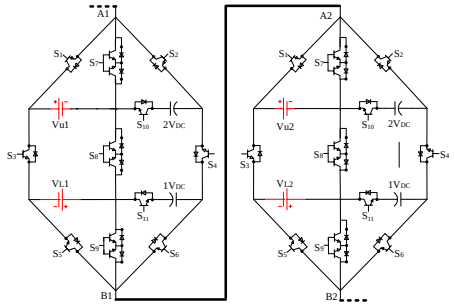

Fig.8 The cascade arrangement of modular proposed multilevel.

TABLE 4
OUTPUT LEVELS FOR TWO MODULES TO CREATE 25 LEVELS

u1= / u2=	**-6**	**-5**	**-4**	**-3**	**-2**	**-1**	**0**	**1**	**2**	**3**	**4**	**5**	**6**
-6	-12	-11	-10	-9	-8	-7	-6	-5	-4	-3	-2	-1	0
-5	-11	-10	-9	-8	-7	-6	-5	-4	-3	-2	-1	0	1
-4	-10	-9	-8	-7	-6	-5	-4	-3	-2	-1	0	1	2
-3	-9	-8	-7	-6	-5	-4	-3	-2	-1	0	1	2	3
-2	-8	-7	-6	-5	-4	-3	-2	-1	0	1	2	3	4
-1	-7	-6	-5	-4	-3	-2	-1	0	1	2	3	4	5
0	-6	-5	-4	-3	-2	-1	0	1	2	3	4	5	6
1	-5	-4	-3	-2	-1	0	1	2	3	4	5	6	7
2	-4	-3	-2	-1	0	1	2	3	4	5	6	7	8
3	-3	-2	-1	0	1	2	3	4	5	6	7	8	9
4	-2	-1	0	1	2	3	4	5	6	7	8	9	10
5	-1	0	1	2	3	4	5	6	7	8	9	10	11
6	0	1	2	3	4	5	6	7	8	9	10	11	12

TABLE 5
OUTPUT LEVELS OF UNITS FOR TWO MODULES TO CREATE 169 LEVELS

u1= / u2=	**-6**	**-5**	**-4**	**-3**	**-2**	**-1**	**0**	**1**	**2**	**3**	**4**	**5**	**6**
-78	-84	-83	-82	-81	-80	-79	-78	-77	-76	-75	-74	-73	-72
-65	-71	-70	-69	-68	-67	-66	-65	-64	-63	-62	-61	-60	-59
-52	-58	-57	-56	-55	-54	-53	-52	-51	-50	-49	-48	-47	-46
-39	-45	-44	-43	-42	-41	-40	-39	-38	-37	-36	-35	-34	-33
-26	-32	-31	-30	-29	-28	-27	-26	-25	-24	-23	-22	-21	-20
-13	-19	-18	-17	-16	-15	-14	-13	-12	-11	-10	-9	-8	-7
0	-6	-5	-4	-3	-2	-1	0	1	2	3	4	5	6
13	7	8	9	10	11	12	13	14	15	16	17	18	19
26	20	21	22	23	24	25	26	27	28	29	30	31	32
39	33	34	35	36	37	38	39	40	41	42	43	44	45
52	46	47	48	49	50	51	52	53	54	55	56	57	58
65	59	60	61	62	63	64	65	66	67	68	69	70	71
78	72	73	74	75	76	77	78	79	80	81	82	83	84

C. Comparative Study

The proposed module (K-Type) aims to get maximum levels from two DC sources. Regarding this issue, there are few configurations with exact two sources to compare, rarely. Thus, the similar new configurations are considered in table 6 for comparative study. Some of these configurations just have DC sources ([12, 24, 25]) without any capacitors to show the reduction of DC source in the proposed module. Some other one involves one DC sources ([18, 35, 36]) to show the reduction of semiconductors in the proposed module. And some other ones are including one DC source and one capacitor in their module ([27, 29]). [34] has two DC sources and some capacitors in its module. [34] can be a close configuration to the K-Type from the number of DC sources aspect in the module. As shown in

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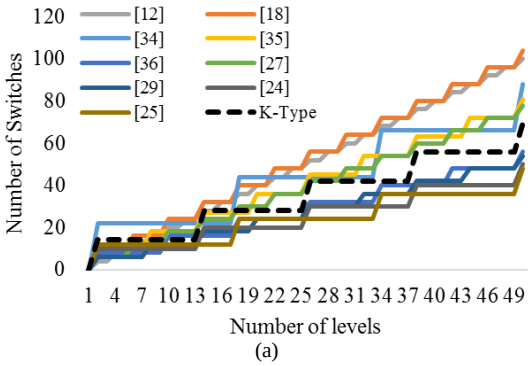
Table 6, a comparative study between the proposed topology and other ones is studied regarding the number of switches, the number of diodes, the number of DC sources, the number of capacitors, TSV and the ability to generate negative voltage level in terms of level numbers.

TABLE 6
COMPARISON OF SOME MODULAR MULTILEVEL INVERTER TOPOLOGY

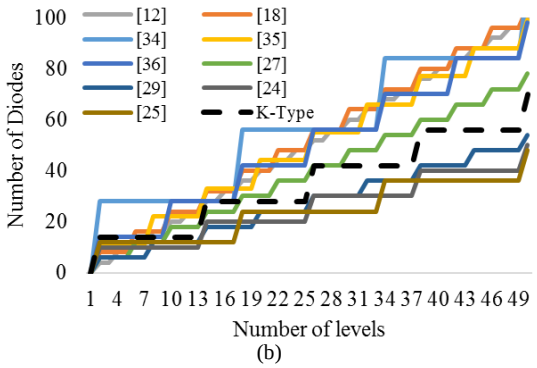
	CHB [12]	[18]	[34]	[35]	[36]	[27]	[29]	[24]	[25]	Proposed module
Number of Switches	$4\left[\frac{N_L-2}{2}+1\right]$	$8\left[\frac{N_L-2}{4}+1\right]$	$22\left[\frac{N_L-3}{16}+1\right]$	$9\left[\frac{N_L-2}{6}+1\right]$	$8\left[\frac{N_L-2}{8}+1\right]$	$6\left[\frac{N_L-2}{4}+1\right]$	$6\left[\frac{N_L-2}{6}+1\right]$	$10\left[\frac{N_L-2}{12}+1\right]$	$12\left[\frac{N_L-3}{16}+1\right]$	$14\left[\frac{N_L-2}{12}+1\right]$
Number of Diodes	$4\left[\frac{N_L-2}{2}+1\right]$	$8\left[\frac{N_L-2}{4}+1\right]$	$28\left[\frac{N_L-3}{16}+1\right]$	$11\left[\frac{N_L-2}{6}+1\right]$	$14\left[\frac{N_L-2}{8}+1\right]$	$6\left[\frac{N_L-2}{4}+1\right]$	$6\left[\frac{N_L-2}{6}+1\right]$	$10\left[\frac{N_L-2}{12}+1\right]$	$12\left[\frac{N_L-3}{16}+1\right]$	$14\left[\frac{N_L-2}{12}+1\right]$
Number of DC sources	$\left[\frac{N_L-2}{2}+1\right]$	$\left[\frac{N_L-2}{4}+1\right]$	$2\left[\frac{N_L-3}{16}+1\right]$	$\left[\frac{N_L-2}{6}+1\right]$	$\left[\frac{N_L-2}{8}+1\right]$	$\left[\frac{N_L-2}{4}+1\right]$	$\left[\frac{N_L-2}{6}+1\right]$	$4\left[\frac{N_L-2}{12}+1\right]$	$4\left[\frac{N_L-3}{16}+1\right]$	$2\left[\frac{N_L-2}{12}+1\right]$
Number of capacitors	-	$2\left[\frac{N_L-2}{4}+1\right]$	$6\left[\frac{N_L-3}{16}+1\right]$	$2\left[\frac{N_L-2}{6}+1\right]$	$3\left[\frac{N_L-2}{8}+1\right]$	$\left[\frac{N_L-2}{4}+1\right]$	$\left[\frac{N_L-2}{6}+1\right]$	-	-	$2\left[\frac{N_L-2}{12}+1\right]$
PIV*	nV_{DC}	nV_{DC}	nV_{DC}	nV_{DC}	nV_{DC}	nV_{DC}	nV_{DC}	nV_{DC}	nV_{DC}	nV_{DC}
TSV** (xV_{DC})	$\left[\frac{N_L-2}{2}+1\right]$	$12\left[\frac{N_L-2}{4}+1\right]$	$88\left[\frac{N_L-3}{16}+1\right]$	$17\left[\frac{N_L-2}{6}+1\right]$	$17\left[\frac{N_L-2}{8}+1\right]$	$8\left[\frac{N_L-2}{4}+1\right]$	$12\left[\frac{N_L-2}{6}+1\right]$	$28\left[\frac{N_L-2}{12}+1\right]$	$39\left[\frac{N_L-3}{16}+1\right]$	$32\left[\frac{N_L-2}{12}+1\right]$
Negative level	With H-Bridge	With H-Bridge	With H-Bridge	With H-Bridge	With H-Bridge	Inherent	Inherent	Inherent	Inherent	Inherent

*Peak Inverse Voltage ** Total Standing Voltages

Fig.9 depicts the parameters versus levels. The Fig.9 is staircase form since the modules would be connected together modularity, and each module provides some range of levels with the same components. According to Fig.9.a and Fig.9.b, the number of switches/diodes in the proposed module is better than the single sources modules, although the DC source modules without capacitor had better performance. It is obvious that the K-type has fewer semiconductors than [34]. In Fig.9.c, proposed configuration uses lower DC source, except for the single source configurations. Moreover, in some levels are the same these configurations (the single source configurations). On the other side, it needs the lowest number of capacitors among with [29] (see Fig.9.d). PIV (Peak Inverse voltage) is the same for all configuration. It also has a reasonable range of TSV like other ones in Fig.9.e. It is noticeable that proposed topology and [27, 29, 24, 25] can generate negative voltage levels which do not need any additional circuit. And [12, 18, 34, 35, 36] can not do it without H-bridge. This ability along with lower components and stress on the devices confirms that the proposed inverter can perform well in comparison with other existing ones.



(a)



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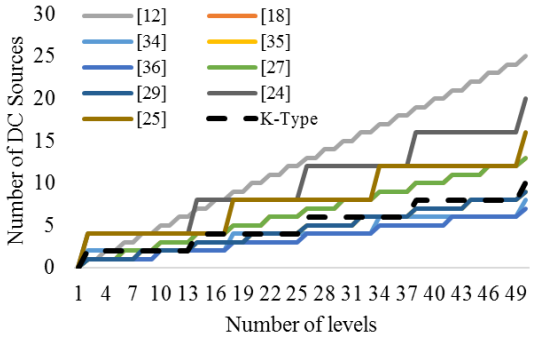

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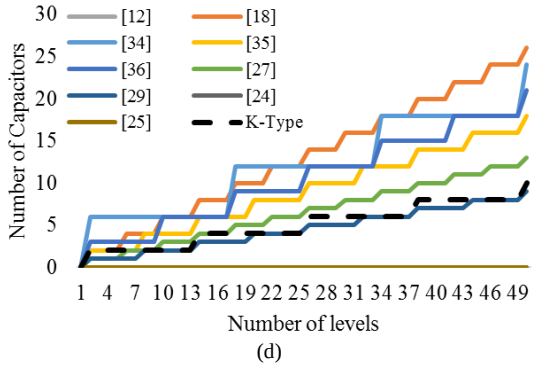

(d)

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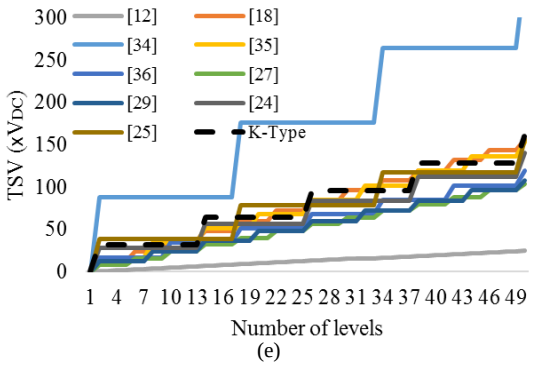

(e)

Fig.9 comparative studies: The number of switches (a), The number of diodes (b), The number of sources (c), The number of capacitors (d), and TSV (e) in terms of number of levels.

III. Nearest Level Control (NLC) Modulation Method

The nearest level control method (NLC) is applied as a simplified switching technique in proposed multilevel [37]. The aim is using NLC method in converters with a high number of levels. It causes simplify the calculation of the processor. Fig.10 depicts the NLC method to describe the algorithm to create a sample staircase multilevel voltage waveform. According to Fig.10.a, the controller samples a point from the reference voltage (V_{ref}) and then round it to the nearest of the voltage level (V_{aN}). Each voltage level has a switching logic according to the switching lookup table (Table 1) to change switches status (Fig.10.b). The sampling can be repeated for each sample time (Ts). In case of multilevel as a voltage source converter, it needs to calculate the steps timing as offline and program the processor for desire waveform due to steps switching are fixed for each level to generate sinusoidal waveform.

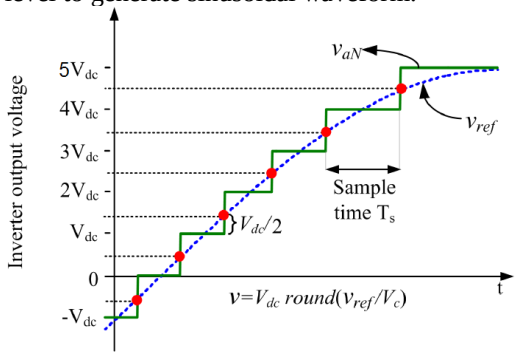

Fig.10 Nearest level control (a) Waveform synthesis (b) Control diagram.

IV. Calculation of Losses

The switching of semiconductor devices produces two major types of power losses: Conductive and switching losses. a comprehensive loss analysis in K-Type is presented as follow:

Conductive losses

Conductive losses (Pc) is in on-state of switches. It is assumed a typical power switch and diode and It can be extended for a multilevel inverter. The losses for a transistor (pc,T(t)) and diode (pc,D(t)) in instantaneous conduction is as follows:

$$pc,T(t) = [V_T + R_T i^{\beta}(t)]\, i(t) \quad (1)$$

$$pc,D(t) = [V_D + R_D i(t)]\, i(t) \quad (2)$$

which V_T and V_D are the voltage of the switch and diode in on-state. R_T and R_D are the resistance of the switch and diode, respectively, and β is a constant specification of the switch. conductive losses of each semiconductor is calculated according to (1) and (2) and add together to calculate total conductive losses of the module.

Switching Losses

The switches waste the power during the switching turn-on and the turn-off as switching loss (Psw). Turn-on and turn-off energy losses (Eon, Eoff) can be considered as follows:

$$E_{off.k} = \int_0^{t_{off}} v(t)i(t)dt = \int_0^{t_{off}} \left[\left(\frac{v_{sw.k}}{t_{off}}t\right)\left(-\frac{I}{t_{off}}(t - t_{off})\right)\right] dt = \frac{1}{6} v_{sw.k} I\, t_{off} \quad (3)$$

$$E_{on.k} = \int_0^{t_{on}} v(t)i(t)dt = \int_0^{t_{on}} \left[\left(\frac{v_{sw.k}}{t_{on}}t\right)\left(-\frac{I'}{t_{on}}(t - t_{on})\right)\right] dt = \frac{1}{6} v_{sw.k} I'\, t_{on} \quad (4)$$

Which $E_{off,k}$ is the turn-off loss for the switch k, t_{off} is the turn-off time, I (I') is the current through the switch before (after) turn-off (on), and $V_{sw,k}$ is the off-state voltage on the switch. $E_{on,k}$ is the turn-on loss for the switch k, t_{on} is the turn-on time of the switch. Thus:

$$P_{sw} = f\left[\sum_{k=1}^{N_{switch}} \left(\sum_{i=1}^{N_{on.k}} E_{on.ki} + \sum_{i=1}^{N_{off.k}} E_{off.ki}\right)\right] \quad (5)$$

Which f is the fundamental frequency, $N_{on,k}$ and $N_{off,k}$ are the number of turning on and off for switch k during a cycle. $E_{on,ki}$ is also the energy loss for the switch k during the i_{th} turn-on and $E_{off,ki}$ is the energy loss for the switch k during the i_{th} turn-off. The total losses of K-Type will be:

$$P_{Loss} = P_C + P_{sw} \quad (6)$$

In the experimental test, following parameters are considered to calculate efficiency of K-Type module:

RT =0.15Ω, VT =2.5 V, RD =0.1Ω, VD =1.5 V, β =1, ton=toff=1 μs, f =50 Hz. Each dc voltage source has the value of 10 V. The resistance of the load is 30 Ω.

The calculation is examined for one cycle by Eqs. (1) to (6). Consequently, the efficiency of K-Type is 95.35% due to low switching frequency for each switch (see Fig.4).

V. The Analysis of Capacitors Ripple

Constant voltages of DC links in the multilevel inverter are most important when the converter is feeding the electrical load. Thus, the voltage ripple in the capacitors should be small (under 5%). There are some parameters to evaluate the capacitor voltage in multilevel converters with capacitors as DC links. Ripple factor (RF) and figure factor (FF) are the parameters which are considered in the analysis of capacitors ripple:

$$RF = \frac{V_{ac}}{V_{dc}} \quad (7)$$

$$FF = \frac{V_{rms}}{V_{dc}} \quad (8)$$

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And,

$$V_{ac} = \sqrt{V_{rms}^2 - V_{dc}^2} \quad (9)$$

The waveform of ripple is considered as a sinusoidal waveform with 6 times more than the fundamental period time since the ripple should not exceed above 5% (see Figures 19 and 20). On the other hand, the drop voltage of capacitors are not lower than $0.95V_{max}$ and the boundaries of below integrals are between 77° and 103°:

$$V_{dc} = \frac{1}{T}\int_{Start\ angle\ of\ ripple}^{End\ angle\ of\ ripple} f(\theta)\ d\theta = \frac{2\times1}{2\pi}\int_{77°}^{103°} V_{max}\sin\frac{\theta}{6}\ d\theta \quad (10)$$

$$V_{rms} = \sqrt{\frac{1}{T}\int_{Start\ angle\ of\ ripple}^{End\ angle\ of\ ripple} f^2(\theta)\ d\theta} = \sqrt{\frac{2\times1}{2\pi}\int_{77°}^{103°} V_{max}^2\sin^2\frac{\theta}{6}\ d\theta} \quad (11)$$

It is obvious, V_{max} for C1 is 10 and for C2 is 20 (see parallel charging in figures 5) According to equations (7) to (11), $Vdc_{,C1}$=9.65 , $Vdc_{,C2}$=19.3 , $Vrms_{,C1}$=9.75 , $Vrms_{,C2}$=19.5 , $Vac_{,C1}$=1.39 , $Vac_{,C2}$=2.78 , and therefore: $FF_{,C1}$=1.01 , $RF_{,C1}$=0.14 and $FF_{,C2}$= 1.01, $RF_{,C2}$=0.14.

This analysis shows the voltage of capacitors are constant and standard to use in presented multilevel inverter.

The amount of capacitors: the determination of capacity for capacitors depends on application load, directly. On the other hand, the capacitors should have ample energy to supply the load during each periodic cycle on their levels (see fig.4). In this case as a numerical example, it is assumed that the AC electrical load consumes 60 watts hour (or 333 microwatts for each 20 millisecond=one cycle). According to Fig.4, the C1 supplies levels -4,-6, 4, 5 and 6 that it means 45 microwatts for each one cycle and the C2 supplies levels -5,-6, 4, 5 and 6 that it also means 80 microwatts for each one cycle. Besides, the drop voltage of the capacitors should not go above 5% to have a standard constant voltages as the DC links. Thus, ΔV_{C1}<0.5 and ΔV_{C2}<1. Energy in capacitors is written as follows:

$$E_C = \frac{1}{2}\ C\ \Delta V^2 \quad (12)$$

Consequently, the amount of the capacitors are calculated and selected as C1≥360μF and C2≥190μF in which the drop voltage in DC links do not exceed above 5% for this case. It is obvious, the ripples will be reduced in DC links with higher capacitors.

VI. SIMULATIONS RESULTS

The proposed multilevel inverter is simulated by MATLAB/SIMULINK to examine the performance of the proposed module. Fig.11.a shows the output voltage of 13-levels for the proposed multilevel inverter with switching technique NLC. Each level (V_{DC}) is 10 volts to create 50 Hz sinusoidal waveform. Fig.11.b also illustrates harmonics spectrums that validate each harmonic order is in low range. THD% is calculated 3.87% by FFT analysis for waveform of Fig.11 which satisfied IEEE519 (THD% ≤ 8% and each order ≤ 5%).

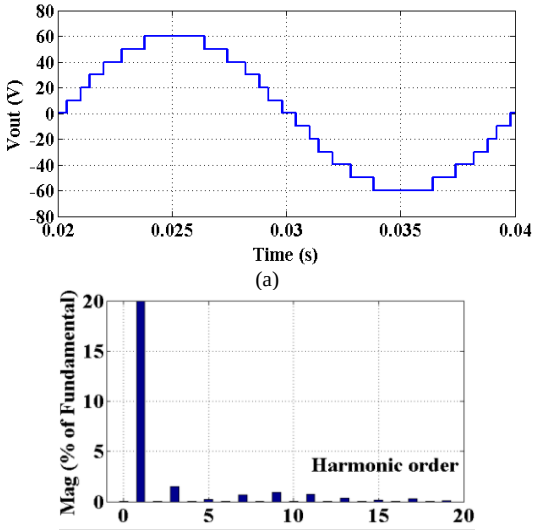

Fig.11 The waveform of output Voltage (simulation) for the proposed module: (a) Waveform (b) Harmonics spectrums.

In addition, Fig.12 and Fig.13 depict the results of the first and the second cascade topology with switching technique NLC. They confirm the performance and modular abilities of proposed topologies as 25 levels with THD=1.99% for the first cascade topology and 169 levels with THD=0.11% for the second cascade topology. Harmonics spectrums figures (Fig.12.b and Fig.13.b) also satisfied IEEE519 in cascade topologies. Cascade topologies have good performance to create waveform similar to the sinusoidal waveform with low harmonics.

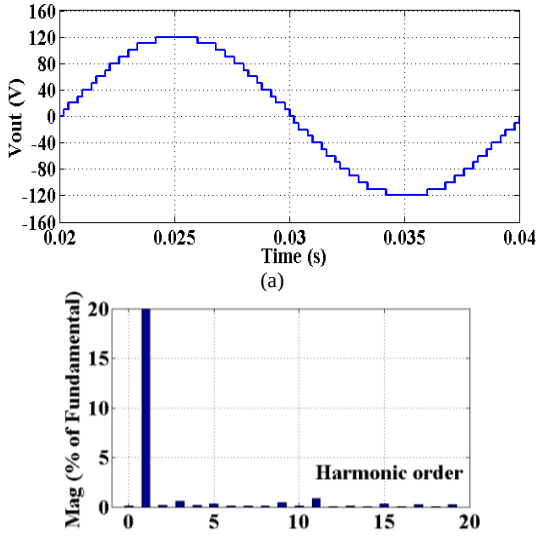

Fig.12 The waveform of output Voltage (simulation) for the first cascade topology (25 Levels): (a) Waveform (b) Harmonics spectrums.

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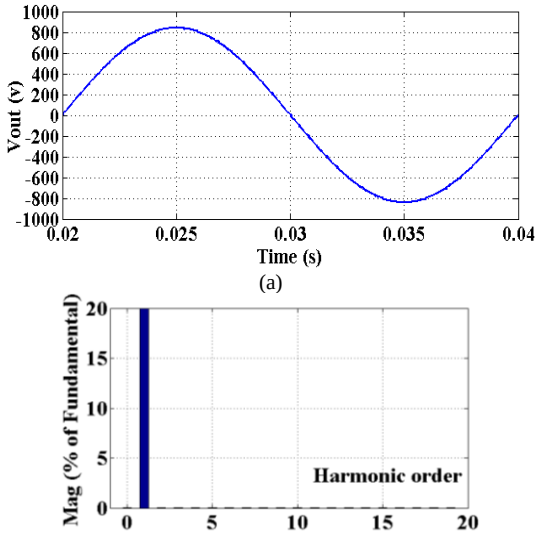

Fig.13 The waveform of output Voltage (simulation) for the second cascade topology (169 Levels): (a) Waveform (b) Harmonics spectrums.

VII. EXPERIMENTAL RESULTS

A prototype setup is fabricated to verify the performance of the proposed module and cascade topology connection. Microcontroller ATMEGA16 are programmed Based on Table 1 and Table 4 for switching pulses, and optocoupler-drivers (HCPL3120) drive MOSFET (23N50E) to produce the sinusoidal waveform with frequency 50 Hz. Fig.14 shows Experimental setup picture in the laboratory.

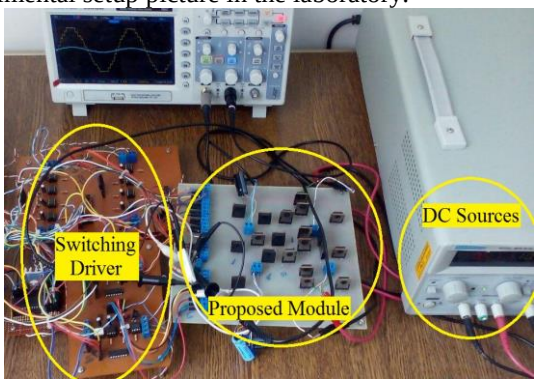

Fig.14 Experimental setup picture in laboratory.

The experimental test on setup system is executed as well as V_{DC} for each step is considered 10 volts. Thus, DC suppliers are set on 10 (V) for $1V_{DC}$ and 20 (V) for $2V_{DC}$ in which $\pm 6xV_{DC}$ and $\pm 12xV_{DC}$ are generated for single module and two module (mode.I), respectively. 13 levels and 25 levels MLI supplies the electrical load. Fig.15 shows voltage and current 50 Hz sinusoidal waveforms of the proposed module for 13 levels in resistive load (30Ω). Fig.16 shows this case in inductive-resistive load (325mH and 30Ω in parallel, COSΦ=0.85) as well. THD is 4.07% for 13 levels in experimental test. Fig.17 and Fig.18 Also depict the results for 25 levels in resistive load (30Ω) and inductive-resistive load (325mH and 30Ω in parallel, COSΦ=0.85), respectively in which THD is 2.26%. The prototype is studied and shown the performance of the proposed module.

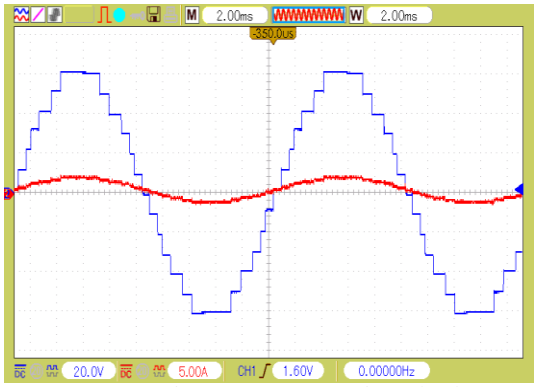

Fig.15 The output voltage of experimental results for 13 levels (COSΦ=1).

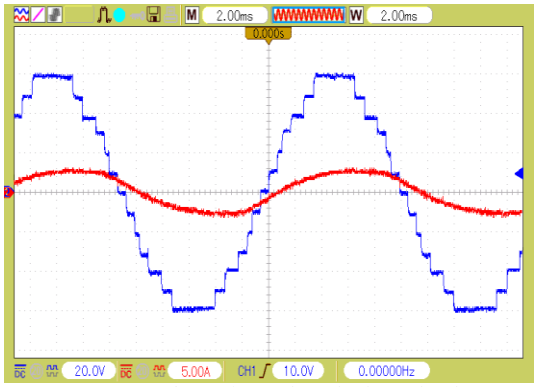

Fig.16 The output voltage of experimental results for 13 levels (COSΦ=0.85).

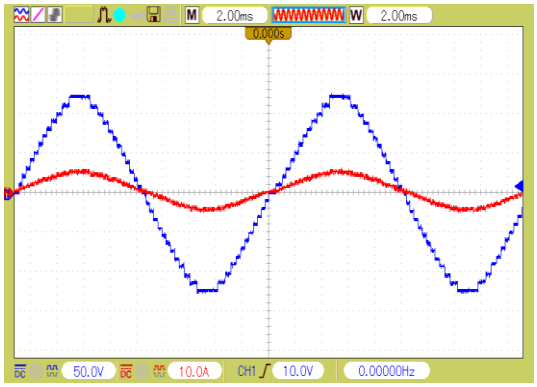

Fig.17 The output voltage of experimental results for 25 (COSΦ=1).

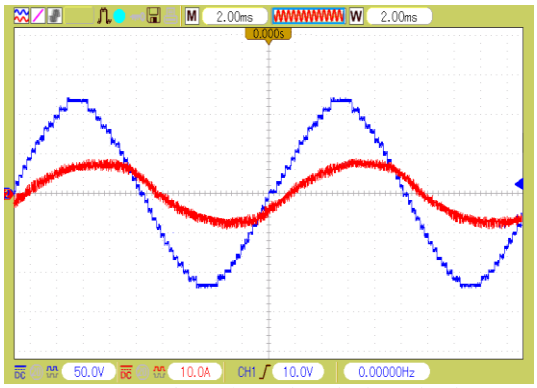

Fig.18 The output voltage of experimental results for 25 levels (COSΦ=0.85).

In the experimental test for the prototype setup the capacity of capacitors (470 microfarad) as enough as to supply the load until the next level zero for charging again. Thus, the character of the capacitors are shown in steady state after the initial

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charging. Fig.19 and Fig.20 demonstrate the voltage of V_{C1} and V_{C2} that is on 10 and 20 volts, respectively.

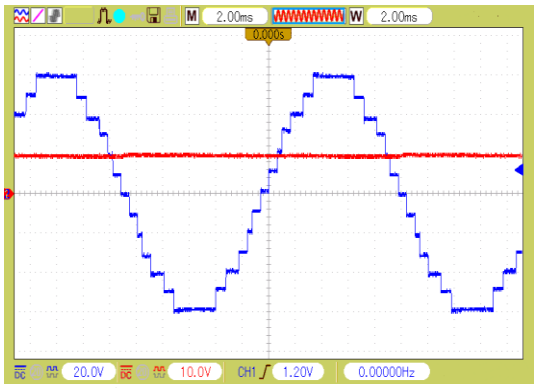

Fig.19 The voltage of V_{C1} experimental results.

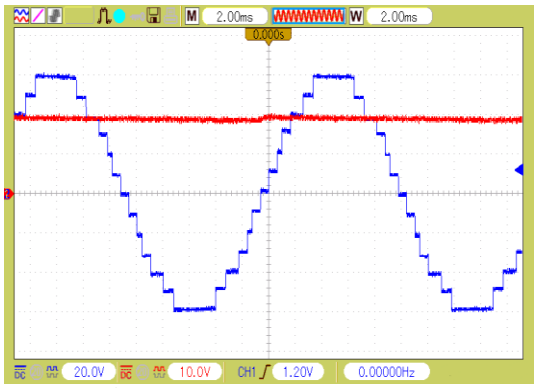

Fig.20 The voltage of V_{C2} experimental results.

VIII. Conclusion

This paper introduced one module for asymmetrical multilevel inverter to produce 13 levels by two DC sources. The proposed multilevel is designed based on two back to back T-Type modules with some switches around them. The proposed module is named K-Type. The configuration of K-type provides two extra DC links by capacitors (as the virtual DC supply) to achieve more levels to create staircase waveform. The module needs lower components including two DC sources, two capacitors, 14 semiconductors. It can be used in power applications with unequal DC sources (with ratio 1:2). It can also be easily modularized in two strategies in cascade arrangements to form high voltage outputs with low stress on semiconductors and lowering the number of devices. This ability can be used in some special applications such as solar farm along with a lot of DC sources. DC sources can also have different voltage amplitudes. In the conventional methods, it should be considered one inverter for each DC resources and fix the output voltage the same amplitude. It increases complexity and losses from this aspect, but in asymmetrical multilevel converters, it is possible to combine some DC resources together and generate a unique AC output. It reduces the number of separated inverter, components, losses and etc. The other advantage of K-Type module is its capability to generate both positive and negative output voltage without any additional circuit. Module is tested and it shows a good performance. THD% for one module is obtained 3.87% and 4.07% in simulation and experimental results, respectively that satisfy harmonics standard (IEEE519). THD% for cascade connection (two module) is calculated 1.99% in simulation and 2.26% in experimental results.

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